Docket Number
36856.1439

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant: Takayuki TSUKIZAWA et al. Application No.: 10/596,312 Confirmation No.: 5223 Filing or 371(c) Date: June 8, 2006 Title: METHOD FOR MANUFACTURING CHIP ELECTRONIC COMPONENT-MOUNTED CERAMIC SUBSTRATE	Art Unit: 3729 Examiner: T. Phan

APPEAL BRIEF UNDER 35 U.S.C. § 134(a)

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Appeal pursuant to 35 U.S.C. § 134(a) from the rejection of Claims 16-22 in the Final Office Action dated November 20, 2009.

REAL PARTY IN INTEREST:

The real party of interest is the assignee, Murata Manufacturing Co., Ltd., 10-1, Higashikotari 1-chome, Nagaokakyo-shi, Kyoto-fu, Kyoto 617-8555, Japan.

RELATED APPEALS AND INTERFERENCES:

Appellant, assignee, and the undersigned attorney of record are not aware of any prior or pending appeals, judicial proceedings, or interferences which may be related to, directly affect, or be directly affected by or having a bearing on the Board's decision in the pending Appeal.

STATUS OF CLAIMS:

Claims 16-25 are pending in this Application.

Claims 16-22 have been at least twice rejected over prior art and are the subject of this appeal.

Claims 23-25 have been withdrawn from consideration by the Examiner.

Claims 1-15 and 26-33 have been canceled.

STATUS OF AMENDMENTS:

Appellant has not submitted any amendment after the Final Office Action dated November 20, 2009.

SUMMARY OF CLAIMED SUBJECT MATTER:

Appellant has provided a concise explanation of the subject matter of independent Claim 16 below, with specific references to the reference characters, paragraph numbers, and the figure numbers of U.S. Application No. 10/596,312 in brackets. Appellant notes, however, that this specific explanation is only by way of example and is not intended to limit Appellant's claimed invention to the specific preferred embodiments described in the specification.

Claim 16

A method for manufacturing a chip electronic component-mounted ceramic substrate [reference character 10 shown in Fig .1A], comprising the steps of:

mounting a chip electronic component [reference character 12 shown in Fig. 1A] including a ceramic sintered compact [reference character 112 shown in Figs. 1B and 2B-2E] defining an element assembly and terminal electrodes [reference characters 112D and 112E shown in Figs. 1B and 2B-2E] on a ceramic green body [reference character 111 shown in Figs. 1B, 2D, and 2E] having conductors [reference character 111C shown in Figs. 1B and 2A-2D] thereon such that the terminal electrodes are brought into contact with the corresponding conductors [discussed in paragraphs [0044] and [0047] to [0050] of the Substitute Specification]; and

firing the ceramic green body [reference character 111 shown in Figs. 1B, 2D, and 2E] having the chip electronic component [reference character 12 shown in Fig. 1A] so as to integrate the conductors [reference character 111C shown in Figs. 1B and 2A-2D] on the ceramic green body [reference character 111 shown in Figs. 1B, 2D, and 2E] with the corresponding terminal electrodes [reference characters 112D and 112E shown in Figs. 1B and 2B-2E] of the chip electronic component by sintering [discussed in paragraphs [0044] and [0051] of the Substitute Specification].

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL:

The Examiner's rejection of Claims 16-22 under 35 U.S.C. § 102(b) as being anticipated by Sakamoto et al. (U.S. 6,228,196).

ARGUMENT:

Appellant has grouped Claims 16-22 together so that Claims 17-22 stand or fall with independent Claim 16. Below, Appellant has only specifically argued that Claim 16 is improperly rejected. However, dependent Claims 17-22 have also been improperly rejected for at least the same or similar reasons that Claim 16 has been improperly rejected.

Appellant's claim 16 recites:

> A method for manufacturing a chip electronic component-mounted ceramic substrate, comprising the steps of:
>
> **mounting a chip electronic component including a ceramic sintered compact defining an element assembly and terminal electrodes on a ceramic green body having conductors thereon such that the terminal electrodes are brought into contact with the corresponding conductors**; and
>
> **firing the ceramic green body having the chip electronic component so as to integrate the conductors on the ceramic green body with the corresponding terminal electrodes of the chip electronic component by sintering**. (emphasis added)

Claims 16-22 are improperly rejected under

35 U.S.C. § 102(b) as being anticipated by Sakamoto et al.

In the Response to Arguments section on pages 2 and 3 of the Final Office Action mailed November 20, 2009, the Examiner stated:

> Applicants assert that the prior art Sakamoto et al. do not teach the limitation of "mounting a chip electronic component including a ceramic sintered compact defining . . ." (Remarks, pages 8 and 9; Claim 16, line 3). In response, the claims are viewed in light of the specification and the claimed limitation "mounting a chip electronic component including a ceramic sintered compact defining . . ." is construed as "mounting a chip electronic component including a whole ceramic sintered compact group (Fig. 1, 1) defining . . ." where the prior art Sakamoto et al at a minimum teach the claimed limitation. Furthermore, with respect to the applicants' remarks on page 8 about the claimed limitation of mounting a chip electronic component without any bonding material not taught by the prior art Sakamoto et al, in response to these remarks, the examiner needs to

> emphasize that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims, which are judged with their broadest reasonable interpretation. Moreover, it appears that Appellants fail to recognize the scope of the claims when judged in view of the prior art Sakamoto et al. (See MPEP 2111 and In re Geuns, 26 USPQ 2nd 1057 (Fed. Cir. 1993)).

Appellant respectfully and strenuously disagrees.

Each of the Examiner's allegations in the Response to Arguments is completely irrelevant to the features and method steps recited in Appellant's Claim 16 and to Appellant's arguments originally presented in the Amendment filed on July 31, 2009. Regardless of the Examiner's interpretation of the features recited in Appellant's Claim 16, Appellant's Claim 16 clearly and specifically requires that a ceramic **sintered** compact be mounted on a ceramic **green** body, and that the ceramic **green** body having the ceramic **sintered** compact mounted thereon be **fired together**. As is extremely well-known in the art, a "green" ceramic is, by definition, a ceramic material before sintering. That is a "green" ceramic material is, by definition, an **unsintered** ceramic material.

In contrast to Appellant's Claim 16, col. 12, lines 49-65 and col. 14, lines 51-54 of Sakamoto et al. disclose:

> A compact block for a capacitor containing **a raw ceramic functional material 10g to be the above-mentioned capacitor 10 and a compact block for an inductor containing a raw ceramic functional material 11g to be the inductor 11** are prepared, respectively.
>
> **The compact block for a capacitor 10g** includes a ceramic dielectric member as the ceramic functional material so as to provide a laminated structure where multi-layer internal conductors 21 **are formed via a raw dielectric sheet 20 containing the ceramic dielectric member**. Terminal electrodes 22 and 23 are formed at end faces of the compact block 10 facing to each other. The internal electrodes 21 are provided such that ones to be connected with the terminal electrode 22 at one side and ones to be connected with the terminal electrode 23 at the other side are arranged alternately as in an internal electrode in a known laminated ceramic capacitor.
>
> …
>
> **With the compact blocks 10g and 11g, and the ceramic green sheets 2g to 8g accordingly obtained, a raw composite compact 1g**

to be the multi-layer ceramic substrate 1 after baking can be produced as follows. (emphasis added)

That is, **none** of the chip electronic components 10-12 of Sakamoto et al. include a ceramic **sintered** compact when they are mounted on/in the ceramic **green unsintered** body 1g. Instead, each of the electronic components 10-12 of Sakamoto et al. include ceramic **green unsintered** sheets when they are mounted on/in the ceramic **green unsintered** body 1g. Then, after the entire ceramic **green unsintered** body 1g, including the electronic components 10-12 comprised of ceramic green sheets, is assembled, the entire ceramic **green unsintered** body 1g is fired to form the sintered multilayer ceramic component.

Thus, Sakamoto et al. certainly fails to teach or suggest the features and method steps of "mounting a chip electronic component including a ceramic sintered compact defining an element assembly and terminal electrodes on a ceramic green body having conductors thereon such that the terminal electrodes are brought into contact with the corresponding conductors" and "firing the ceramic green body having the chip electronic component so as to integrate the conductors on the ceramic green body with the corresponding terminal electrodes of the chip electronic component by sintering" as recited in Appellant's Claim 16.

On the Continuation Sheet of the Advisory Action dated March 8, 2010, the Examiner alleged, "Sakamoto et al. do provide several teachings or suggestions for an ordinary skill in the art to apply to the claimed invention. In one suggestion, Sakamoto et al. do teach a preliminary baking of a passive component before its burial into the green sheets (Col. 10, lines 46-49)." Appellant respectfully disagrees.

Col. 10, lines 44-52 of Sakamoto et al. disclose, "Moreover, in these aspects of the present invention, **if the passive component is provided as the compact block, since a raw composite compact with the raw compact block buried therein is baked, compared with the case of baking in the state with a preliminarily baked passive component buried therein, the need of strictly administrating the contraction behavior at the time of baking can be eliminated**, and thus the selection

range of the material to be used in a ceramic green sheet to be the laminated member can be widened" (emphasis added).

In other words, col. 10, lines 44-52 of Sakamoto et al. clearly and specifically discloses that the invention of Sakamoto et al. includes **a raw green unsintered** composite compact with **a raw green unsintered** compact block buried therein that is baked, and definitely does not teach or suggest that the invention of Sakamoto et al. could or should include a previously baked passive component buried therein.

In fact, col. 10, lines 44-52 of Sakamoto et al. clearly and specifically discloses that the invention of Sakamoto et al. does not and should never include a preliminary baked passive component buried in a raw green unsintered composite compact because the combination of the preliminary baked passive component buried in the raw green unsintered composite compact is undesirable due to the requirement to strictly administrate the contraction behavior at the time of baking. That is, Sakamoto et al. clearly teaches away from mounting a ceramic sintered compact on or in a ceramic green unsintered body, and then firing the entire ceramic green unsintered body including the ceramic sintered compact therein as recited in Appellant's Claim 16.

As the Examiner should be well aware, a "claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Because Sakamoto et al. fails to teach or suggest at least the features and steps of "mounting a chip electronic component including a ceramic sintered compact defining an element assembly and terminal electrodes on a ceramic green body having conductors thereon such that the terminal electrodes are brought into contact with the corresponding conductors" and "firing the ceramic green body having the chip electronic component so as to integrate the conductors on the ceramic green body with the corresponding terminal electrodes of the chip electronic component by sintering," Sakamoto et al. clearly fails to anticipate Appellant's Claim 16.

Accordingly, Appellant respectfully reconsideration and withdrawal of the rejection of Claim 16 under 35 U.S.C. § 102(b) as being anticipated by Sakamoto et al.

Appellant further submits that the rejection of Claims 16-22 under 35 U.S.C. § 102(b) as being anticipated by Sakamoto et al. should be reversed, and that Claims 16-22 are allowable, at least for the reasons discussed above. In addition, Appellant respectfully requests that the Examiner rejoin and allow non-elected Claims 23-26 which depend upon generic Claim 16, and is therefore allowable for the reasons that Claim 16 is allowable.

Respectfully submitted,

Dated: May 26, 2010

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CLAIMS APPENDIX:

Claims 1-15 (canceled).

Claim 16 (previously presented): A method for manufacturing a chip electronic component-mounted ceramic substrate, comprising the steps of:

mounting a chip electronic component including a ceramic sintered compact defining an element assembly and terminal electrodes on a ceramic green body having conductors thereon such that the terminal electrodes are brought into contact with the corresponding conductors; and

firing the ceramic green body having the chip electronic component so as to integrate the conductors on the ceramic green body with the corresponding terminal electrodes of the chip electronic component by sintering.

Claim 17 (previously presented): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 16, wherein the ceramic green body is defined by a ceramic green sheet, and a green ceramic stack formed by stacking the ceramic green sheet having the chip electronic component and other ceramic green sheets is fired.

Claim 18 (previously presented): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 17, further comprising the step of:

forming a constraining layer on at least one of an uppermost layer and an internal layer of the green ceramic stack; wherein

the constraining layer primarily includes a sintering-resistant powder that is not substantially sintered at the sintering temperature of the ceramic green sheets.

Claim 19 (previously presented): The method for manufacturing a chip electronic

component-mounted ceramic substrate according to Claim 18, wherein the constraining layer is a sheet including the sintering-resistant powder and an organic binder.

Claim 20 (previously presented): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 19, wherein the sheet of the constraining layer is formed on the uppermost layer of the green ceramic stack, and the method further comprises the step of pressure-bonding the constraining layer to press the chip electronic component into the ceramic green sheet.

Claim 21 (previously presented): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 20, wherein the green ceramic stack having the constraining layer is fired with a pressure of about 0.1 MPa to about 10 MPa being applied thereto.

Claim 22 (previously presented): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 18, wherein the constraining layer is formed of a green compact of the sintering-resistant powder on the uppermost surface of the green ceramic stack.

Claim 23 (withdrawn): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 16, further comprising the step of:

forming a constraining layer in a sheet form having via conductors arranged corresponding to the terminal electrodes of the chip electronic component, on the ceramic green body to form the conductors; wherein

the constraining layer includes a sintering-resistant powder that is not substantially sintered at the sintering temperature of the ceramic green body and an organic binder.

Claim 24 (withdrawn): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 16, wherein the chip electronic component is mounted on the conductors of the ceramic green body with an organic adhesive disposed therebetween.

Claim 25 (withdrawn): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 16, wherein the ceramic green body is defined by a ceramic green sheet primarily including a low-temperature co-fired ceramic powder, and the terminal electrodes of the chip electronic component and the conductors on the ceramic green sheet are formed of an electrode material primarily including at least one of silver, copper, and gold.

Claims 26-33 (canceled).

EVIDENCE APPENDIX:

None.

RELATED PROCEEDINGS APPENDIX:

None.